Design and FPGA Implementation of Two-Dimensional Discrete Wavelet Transform Architectures Using Raster-Scan Method

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Abstract

In this paper, an FPGA implementation of a 2-dimenional discrete wavelet transform (2-D DWT) is proposed to efficiently construct the corresponding two-dimensional architecture by using the raster-scan image method for any given hardware architecture of one dimensional (1-D) wavelet transform filter. The proposed method is based on lifting scheme architecture. The resulting architectures are simple, modular and regular for computation of one or multilevel 2-D DWT. These architectures perform both low pass and high pass filter with multiplierless coefficients calculation. In addition they require a small on-chip area to download the architectures on FPGA Board (Spartan-3E). The proposed 2-D architecture consists of: external memory, Row 1-D arithmetic module, column 1-D arithmetic module and internal memory unit. The row and column 1-D arithmetic units are designed utilizing Biorthogonal filters (5/3 and 9/7).

Keywords: 2-D DWT, FPGA implementation, Lifting scheme architecture, Raster-scan method.

التصميم والتنفيذ باستخدام FPGA للتحويل المويجي المتقطع ذي البعدين بطريقة المسح النقطي

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الخلاصة

في هذه البحث، تم اقتراح تنفيذ بنية التحويل المويجي المتقطع ذي البعدين (2-D DWT) بإستخدام FPGA بكفاءة من خلال أسلوب صورة المسح النقطي لأي بنية مادية للتحويل المويجي ذات البعد الواحد (1-D). وتستند الطريقة المقترحة على معمارية مخطط الرفع. البنية الناتجة كانت بسيطة ونموذجية ومنتظمة لحساب مستوى واحد أو عدة مستويات من التحويل المويجي المتقطع ذي البعدين (2-D DWT)، هذه البنية يمكنها تنفيذ عمليات مرشح الإمرار الواطيء ومرشح الإمرار العالي مع إجراء الحساب للمعاملات بدون مضارب. وبالإضافة إلى ذلك فإنها تتطلب مساحة صغيرة على رقاقة FPGA نوع (Spartan-3E). يتكون الهيكل ذي البعدين المقترح من: الذاكرة الخارجية ووحدة حساب الصف ذات البعد الواحد ووحدة حساب العمود ذات البعد الواحد بالإضافة الى وحدة الذاكرة الداخلية ذات البعد الواحد المصممة للصف والعمود باستخدام مرشحات (5/3 و 9/7) ثنائية التعامد.

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1. Introduction

The discrete wavelet transform (DWT) is developed as an effective tool for multiresolution analysis since its first presentation by Mallat [1] due to its good time-frequency characteristics. The DWT is widely used for signal and image analysis. The direct implementation of DWT usually requires heavily arithmetic computations because it is essentially a two-channel filter bank (i.e. convolution method). Lifting scheme is latest efficient way to reduce the arithmetic complexity and to provide an in place implementation [2]. For 2-D DWT, there are many VLSI architectures [3] - [7]. The direct method of 2-D DWT architecture performs 1-D DWT on the every row and then on every column of the image. However, this architecture needs a frame buffer as shown in Fig .1 which is usually an off –chip to store the intermediate data [8]. The external memory access consumes the most power in the 2-D DWT hardware implementation. The systolic architecture may be preferred because of the smaller external memory access. But this architecture requires some internal line buffer and processing elements which increase the die area and control complexity [6]. In this paper, a simple method is proposed to implement separable 2-D raster-scan image architectures to solve the problem of internal memory access.

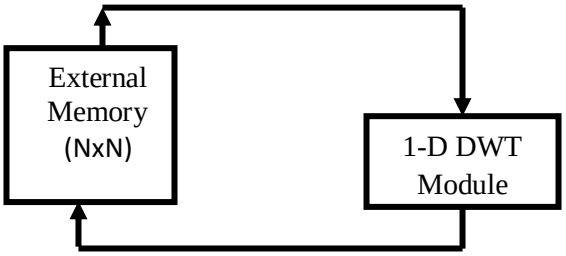

Fig. (1): The direct architecture to perform 2-D DWT.

The basic idea is based on utilizing 2-Data buffer to store the approximation and detail coefficients. These architectures are flexible and can be used for many filter kinds. Based on lifting scheme method**,** a 1-D arithmetic module is used to build the 2-D DWT for one and multilevel transformation. The 2-D DWT architectures are designed to perform the one and multilevel using biorthogonal 5/3 filter & 9/7 filters.

The rest of this paper is organized as follows; The lifting scheme analysis is given in section 2. The 1-D arithmetic modules for 5/3 and 9/7 filters are presented in section 3. In section 4, the proposed architectures are explained. The simulation result and hardware requirement are illustrated in section 5 and 6, respectively. The comparison of the proposed architectures with other architectures of recent studies is shown in section 7. Finally, section 8 concludes this paper.

2. Lifting-Based DWT

The lifting schemes consist of 3-steps as shown in Fig. 2 [9]:

1- **Split step**: - the input signal is separated into even and odd samples.
2- **Predict step**: - the even samples are multiplied by the time-domain equivalent of t(z) and then added to odd samples.
3- **Update step: -** the predict samples are multiplied by time-domain equivalent s (z) and then added to even samples.

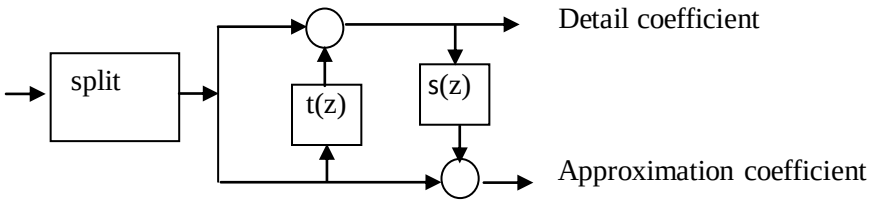

Fig. (2): The Lifting scheme s...

The basic principle of the lifting scheme is to factorize the polyphase matrix of wavelet filter into a sequence of alternating upper and lower triangular matrices and diagonal matrices [9]. The corresponding polyphase matrices are defined by the following matrix equation [4]:

$$\tilde{P}(z)=\prod_{k=1}^{n}\begin{bmatrix}1 & s(z)\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ t(z) & 1\end{bmatrix}. \quad (1)$$

$\tilde{P}(z)$ is defined as polyphase matrix of decomposition stages.

2.1 Lifting scheme for 5/3 filter

The filter coefficients of 5/3 filter are defined as [10]
Low pass decomposition filter *h(n)* = [-1/2 1 -1/2] .
High pass decomposition filter *g(n)* = [-1/8 1/4 3/4 1/4 -1/8] .
The polyphase matrix of the above filter is

$$\tilde{P}(z)=\begin{bmatrix}-1/8\,Z+3/4-1/8\,Z^{-1} & 1/4+1/4\,Z\\ -1/2-1/2\,Z^{-1} & 1\end{bmatrix}$$

$$\tilde{P}(z)=\underbrace{\begin{bmatrix}1 & 1/4\,(1+Z)\\ 0 & 1\end{bmatrix}}_{\text{Update step}}\underbrace{\begin{bmatrix}1 & 0\\ -1/2(1+Z^{-1}) & 1\end{bmatrix}}_{\text{Predict step}} \quad (2)$$

So the approximation and detail coefficients are respectively defined by [13]

$$d(2n+1)=x(2n+1)+\alpha[x(2n)+x(2n+2)] \quad (3)$$

and

$$a(2n)=x(2n)+\beta[d(2n+1)+d(2n-1)] \quad (4)$$

where α = - 1/ 2 , β = 1/ 4 .

2.2 Lifting scheme for 9/7 filter

For a 9/7 symmetric biorthogonal perfect reconstruction (PR) filter, h (k) = h (-k) and g(k)=g(-k); for k = 0; 1; 2; 3; 4 . [11]. Then the even and the odd parts of them can be written as

$$h_e(z)=h(0)+h(2)(z+z^{-1})+h(4)(z^2+z^{-2}) \quad (5a)$$

and

$$h_o(z)=h(1)(1+z)+h(3)(z^2+z^{-1}) \quad (5b)$$

with

$$g_e(z)=-h_o(z^{-1}) \quad (6a)$$

and

$$g_o(z)=h_e(z^{-1}) \quad (6b)$$

2.2.1 Lifting factorization of the 9/7(PR) filter

(i) When $h(3) \neq 0$. [11]

By virtue of Euclidean algorithm, let

$$he(z)=h_o(z)*q_1(z)+r_1(z) \quad (7)$$

then we have

$$(a) \quad q_1(z)= s_0(1 + z^{-1}); \; r_1(z)= t_1(z + z^{-1})+ t_0 \quad (8)$$

where

$s_0=h(4)/h(3)$

$t_0 = h(0) – [2\, h(1)*h(4)]/h(3)$

and

$t_1= h(2) - h(4)-[3h(1)*h(4)]/h(3)$.

$$(b) \quad h_o(z)= r_1(z)*q_2(z) + r_2(z)$$

$$q2(z) = s1(1+ z)$$

$$r_2(z) = t_2(z + 1) \quad (9)$$

where

$s_1 =h(3)/t_1$

and

$t_2 = h(1) - h(3) – [t0*h(3)] /t_1$

$$(c) \quad r_1(z)= r_2(z)*q_3(z) + r_3(z) \quad (10)$$

Also

$$q_3(z) = s_2(1 + z^{-1}), \; r3(z) = t_3 \quad (11)$$

where

$s_2 =t_1/t_2$

$t_3 = t_0 - 2t_1$

$$(d) \quad r_2(z)=t_3*s_3(z+1) \quad (12)$$

and

$$q_4(z)=s_3(1+ z), \; r_4(z)= 0 \quad (13)$$

where

$s_3 =t_2/t_3$.

The above process can be summarized as in the following lifting factorization, where the polyphase matrix of the decomposition stage is defined as

$$\tilde{P}(z) = \begin{bmatrix} h_{0e}(z) & h_{0o}(z) \\ g_{1e}(z) & g_{1o}(z) \end{bmatrix} \quad (14)$$

The above equation can be rewritten as

$$\tilde{P}(z) = \begin{bmatrix} 1 & s_0(1+z^{-1}) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ s_1(1+z^{-1}) & 1 \end{bmatrix} \begin{bmatrix} 1 & s_2(1+z^{-1}) \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ s_3(1+z^{-1}) & 1 \end{bmatrix} \quad (15)$$

2.2.2 Construction of the 9/7 wavelet filter

It is necessary to point out that, for any given filter coefficients h(k)= h(-k) and g(k)=g(-k); [11] they need not be wavelet filters. In fact, in order to achieve the 9/7 wavelet filter, may be calculated using the vanishing moments that satisfy M =2 and M□□ = 4, can be calculated using

$h^{(k)}(z)|_{z=-1}=0$, k=0,1 and

$g^{(k)}(z)|_{z=-1}=0$, k=0,1,2,3

Rewriting (15) as

$$\tilde{P}(z)=\begin{bmatrix}1 & \alpha(1+Z^{-1})\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ \beta(1+Z) & 1\end{bmatrix}\begin{bmatrix}1 & \gamma(1+Z^{-1})\\ 0 & 1\end{bmatrix}\begin{bmatrix}1 & 0\\ \delta(1+Z) & 1\end{bmatrix}\begin{bmatrix}\xi & 0\\ 1 & 1/\xi\end{bmatrix} \quad (16)$$

Based on the vanishing moments conditions and normalization conditions h(1) = 2; g(1)= 1, and comparing (15) and (16), different coefficients can be evaluated as

$\alpha = (-2t+1)/4(t-1)$
$\beta = -(t-1)^2$
$\gamma = 1/(4t(t-1))$
$\delta = t^3 - (7t^2/4) + t\zeta = 2/t$ (17)

From (16) and (17), symmetric biorthogonal 9/7 filters can be obtained with a free variable t. In other words, for any real parameter t, (16) and (17) can be used for signal decomposition, where h and $\tilde{h}$ denote low pass filters, and g and $\tilde{g}$ denote high pass filters for analysis and synthesis, respectively. In order to achieve the 9/7 symmetric biorthogonal wavelet filter, Daubechies's theorem can be employed to determine the interval that the parameter t (z) can be included. Firstly, denote h_9 (z) and $\tilde{h}_7$ (z) by [11]

$$h_9(z) = ((1+z^{-1}/2))^2\ F(z) \quad (18)$$

$$\tilde{h}_7(z) = ((1+z^{-1}/2))^2\ Q(z) \quad (19)$$

Taking t =1.25; then the coefficients of the 9/7 wavelet filter are given by

{h(0), h(1), h(2), h(3), h(4)} = (1/10) x{190/16, 86/16, 24/16, 6/16, 9/16}

{g(0), g(1), g(2), g(3)} = {18/32, 19/64, -1/32, -3/64}

h(-k) = h(k) .

g(-k) = g(k) . (20)

3. The Proposed Arithmetic Module

3.1 1-D arithmetic module

The proposed architecture contains the two dimensional forward discrete wavelet transform (2-D FDWT) and the two dimensional inverse discrete wavelet transform (2-D IDWT). It calculates in row –column fashion on the NXN image by using Biorthogonal filters (5/3 & 9/7 filter)). Such architecture consists of: Row 1-D DWT arithmetic module, memory unit, and column 1-D DWT arithmetic module, Note that the forward discrete

wavelet transform (FDWT) and the inverse discrete wavelet transform (IDWT) are symmetrical. In the remaining parts of this paper, all the details are discussed in terms of discrete wavelet transform modeling by using (5/3, 9/7) filters.

3.1.1 1-D DWT arithmetic module for 5/3 filter

The 1-D DWT module of lifting scheme can be naturally pipelined as shown in Fig. 3 [13].

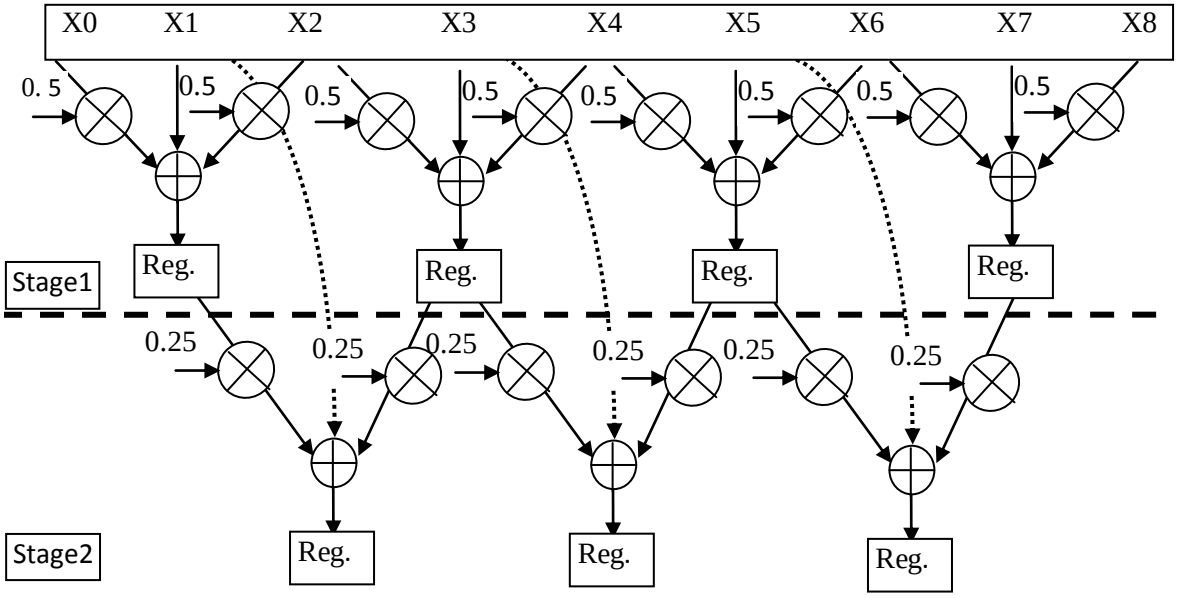

Fig. (3): 1-D DWT Module in 5/3 filter by using multiplier.

Since such module uses multipliers and adders, another 1-D DWT arithmetic module using pipelining of shift integer adder is proposed as shown in Fig. 4. The pipeline structure reduces the area cost of the architecture as compared with the multiplier arithmetic module and reduces the worst delay path between registers.

The proposed 1-D DWT arithmetic module in 5/3 filter consists of two stages; the first stage is used to calculate the detail coefficient and the second stage calculates the approximation coefficient as shown in Fig. 5. So each stage has three input signals and two data output signals.

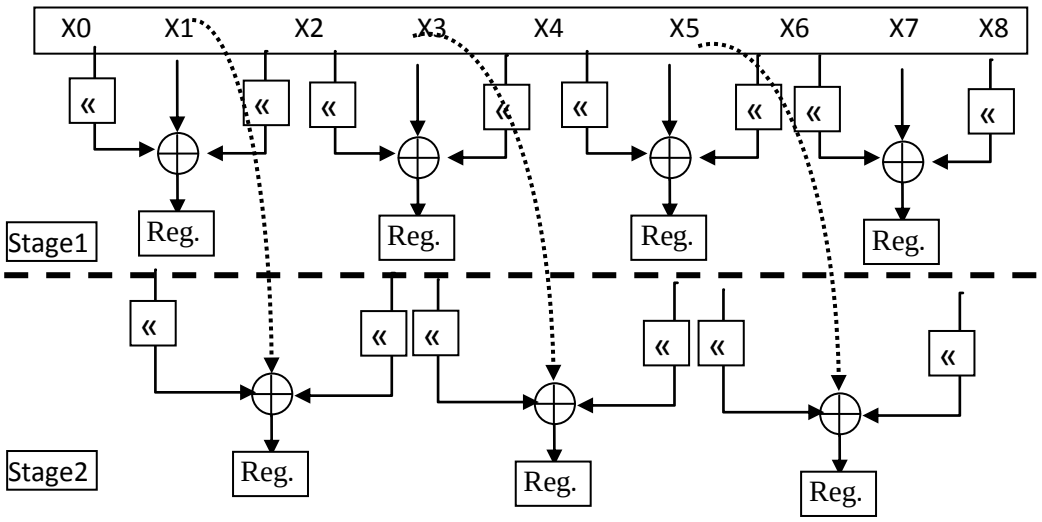

Fig. (4): 1-D DWT arithmetic module in 5/3 filter by using shift integer- adder.

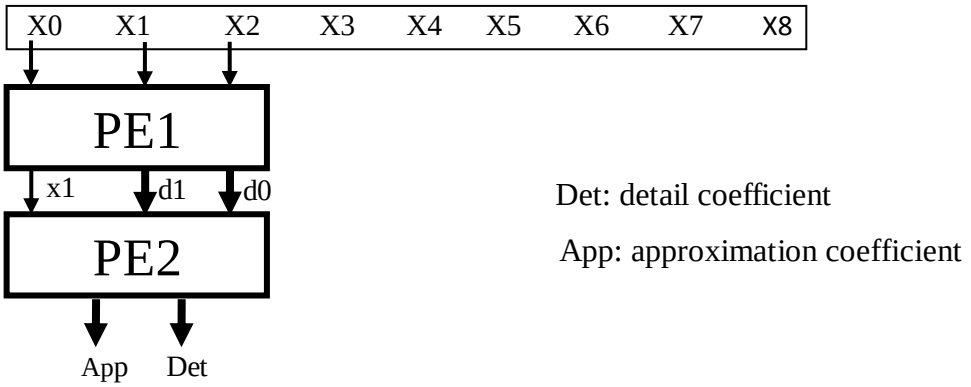

Fig. (5): The processing elements (PE's) of 1-D DWT arithmetic Module in 5/3 filter.

3.1.2 1-D DWT arithmetic module for 9/7 filter

In this paper, the 9/7 filters are designed as 4-stage pipelined shift integer adder without using any multipliers as shown in the Fig. 6. Depending on equation (9). So the 9/7 filter can be designed as two blocks, each block is a 5/3 filter pipelined –shift integer adder module with a simple change in block 1 as shown in Fig. 7.

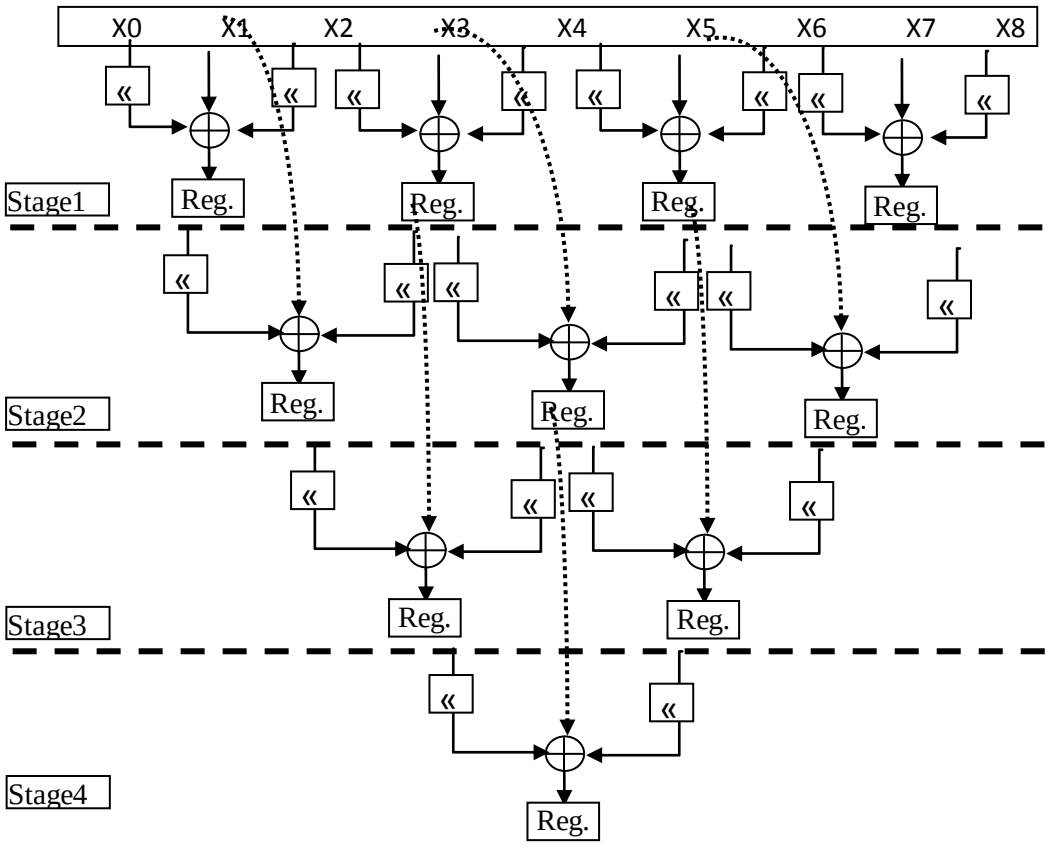

Fig. (6): 1-D DWT arithmetic Module in 9/7 filter.

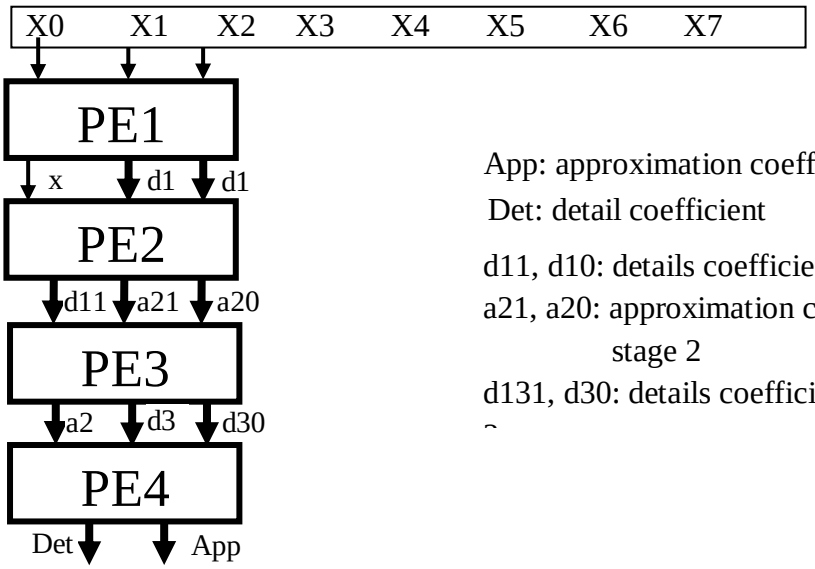

Fig. (7): The 9/7 filter as two blocks of 5/3 filter.

In 5/3 filter, the 1-D DWT arithmetic module consists of three input signals and two output signals, In 9/7 1-D DWT arithmetic module, block 1 consist of three input signals and three output signals, while the block2 in 9/7 module, is exactly the arithmetic module in 5/3 filter. So, the 1-D DWT arithmetic module in 9/7 filter can be designed using two 1-D DWT arithmetic modules in 5/3 filter as shown in Fig. 8.

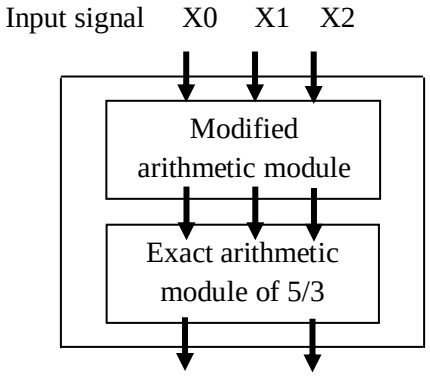

Fig. (8): The 9/7 filter design based on 5/3 filter.

4. The Proposed FPGA Implementation

4.1 The proposed 1-level architectures

The proposed architecture performs 2-D DWT on the input signal (image) by using row-column fashion, so it is required to use three arithmetic modules to calculate the lifting scheme. One of these arithmetic modules is used to calculate the 1-D DWT for each row in the image and the others are used to calculate the 1-D DWT for each column in the image.

As shown in Fig. 9, The input data (image NXN) must be read as raster scan (i.e. row by row) from external memory, the first row of the image is read from an external memory and stored in the Memory unit 1 (MEM1). After that, the row 1-D arithmetic module of 5/3 filter (block 1) reads three input signals from MEM1, calculates the approximation and detail coefficients and stores the results in MEM2. These operations are repeated until the last pixel of the first row. The second row of the image is stored in MEM1 and the row 1-D arithmetic module of 5/3 filter performs the same operations to calculate the approximation and the detail coefficients of the second row which are stored in MEM3 as shown in Fig. 9. Note that the column 1-D arithmetic module2 (block2) and column 1-D

arithmetic module3 (block3) are not used until this time. When first two coefficients are stored in MEM3, block2 and block3 begin to work by performing the lifting scheme on every column of the image. Block2 reads the approximation coefficients from MEM2 and MEM3 and calculates the sub-band images (LL, LH) and block3 reads the detail coefficients from MEM2 and MEM3 to calculate the sub-band images (HL, HH). Such operations continue until the last pixel of the image. The same structure of Fig. 9 can be used for 9/7 filters, where each of block1, block2 and block3 are replaced by the corresponding 1-D arithmetic module of 9/7 filter instead of the shown 5/3 module.

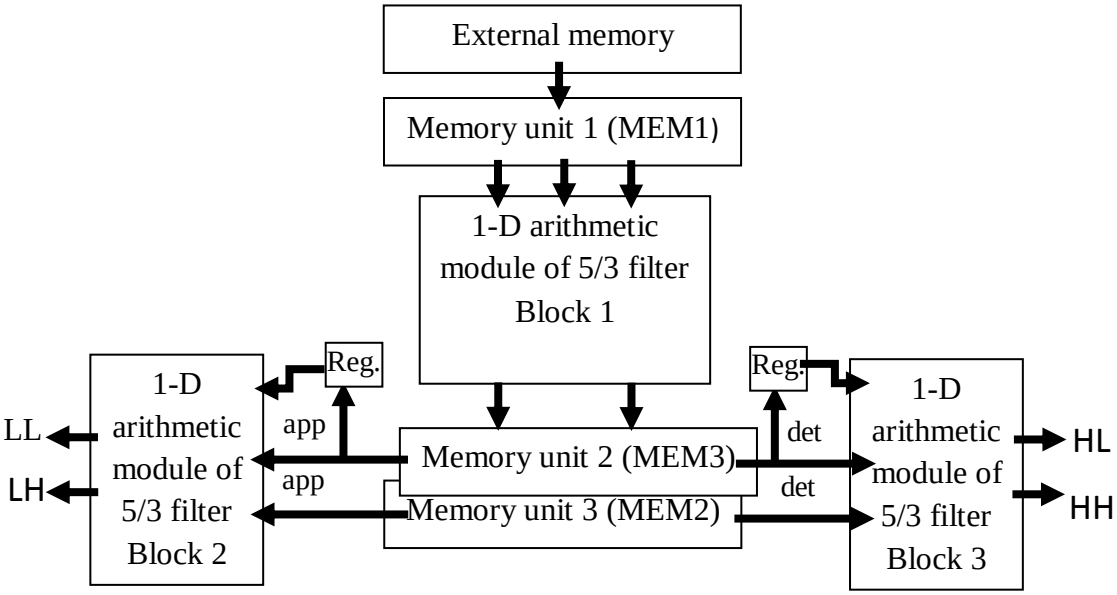

Fig. (9): A one level raster-scan 2-D DWT architectures by using 5/3 filter.

4.2 The proposed multilevel architectures

The proposed 1-level architectures can be easily extended to the multilevel architectures by using the following two methods:

Method 1:- using the proposed 1- level architecture and storing, LL sub-band image in an external memory. When the first level finishes, the same processing element (1- level proposed architecture) reads the LL sub-band image. This process needs the use of the external memory. This will increase the time delay and increase the external memory access but the die area need to build this method will be small.

Method 2:- using n-time of the 1- level proposed architecture, where n is the number of levels. In this paper, the architectures are designed via this method to perform the 3-level 2-D DWT. This method needs a die area in FPGA board greater than the method 1, but method 2 reduces the external memory access and the output from level 2 and level 3 can be used immediately. The multilevel architecture for method 2 is as shown in Fig. 10.

5. Simulation Results

In order to determine the number of bits required for representing each signal, two lengths must be determined. The length of real part (m1) and the length of mantissa part (m2) as shown in Fig. 11. The number of bits for mantissa representation turns out to be the critical parameter for the design. In the proposed architectures, to find the minimum

values of m1 and m2 with reasonable high image quality as shown in Table 1, a Matlab code for a set of standard images is performed. From Table 1, the real part consists of 8 bits in both (5/3 filter and 9/7 filter) architectures, but the mantissa part in (5/3 filter) architectures is 4 bits and the mantissa part in (9/7 filter) is 9 bits.

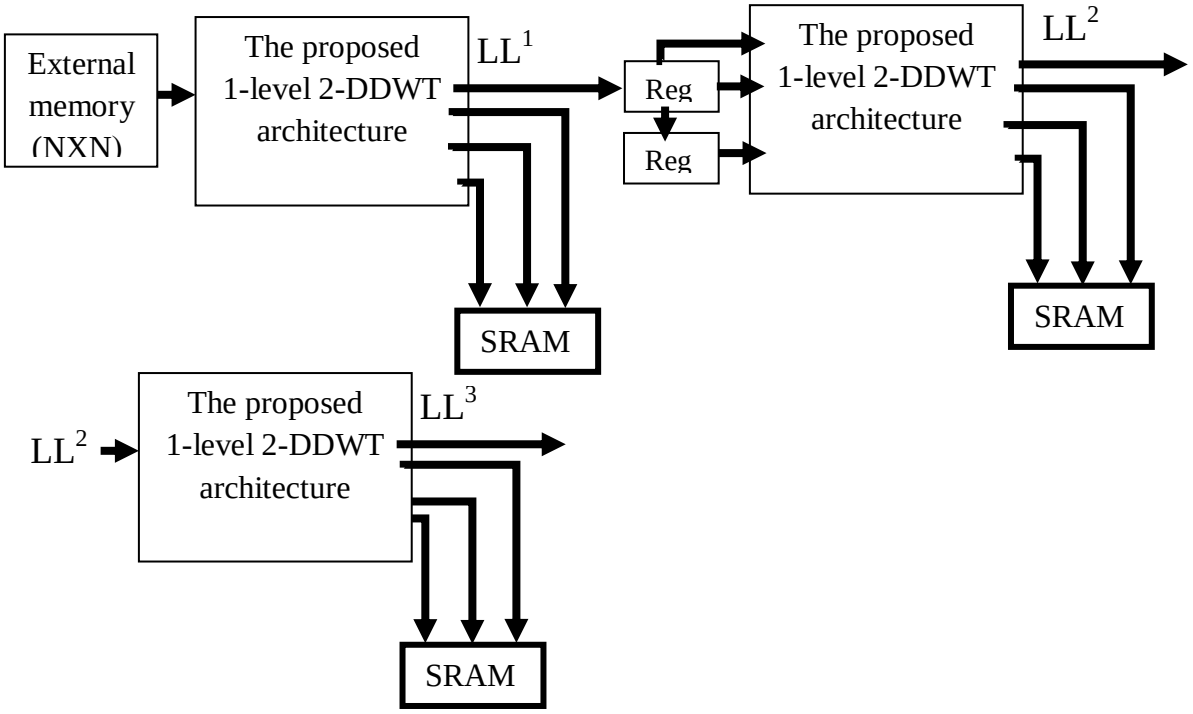

Fig. 10 The proposed multilevel architecture.

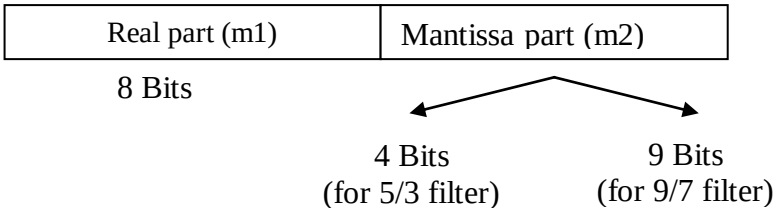

Fig. 11 The total number of bits required for representing each signal for 5/3 and9/7filtrs.

Table 1 The most proper SNR values to determine the total number of bits.

Images	Filter	SNR (dB)
Lena 512 X512	5/3 filter	50
	9/7 filter	39
Barbara 512X 512	5/3 filter	50
	9/7 filter	36
Goldhill 512X512	5/3 filter	50
	9/7 filter	36

6. Hardware Implementation

After achieving satisfactory results from Matlab simulation in the previous section, we proceed to the next stage where the codes are translated into VHDL. Then, the VHDL codes are synthesized using the synthesis tool, which produces "gate level" architecture for VLSI implementation. Finally, the design is down loaded into the FPGA board (Spartan-3E) for the functionality verification. The synthesis results are presented in Table 2.

Table (2): The die area and the max. frequency required for the design of the proposed architectures.

Architectures	Available slices	Number of slices	Max. frequency
Proposed 1-level 2D DWT for 5/3 filter	46	4656	196 MHz
Proposed 1-level 2D DWT for 9/7 filter	57	4656	178.3 MHz
Proposed multilevel (3 levels) architecture for 5/3 filter	210	4656	96.4 MHz
Proposed multilevel (3 levels) architecture for 9/7 filter	285	4656	100.2 MHz

7. A Comparative Study

The proposed design can implement a 2-D multilevel lifting scheme discrete wavelet transform concurrently. It does not use any external memory to store the intermediate results. This will avoid the delay caused by the memory access. As illustrated in Table 3, the design of 1-level of raster-scan 2-D DWT architecture for 5/3 filter requires 12 adders and 9 shift registers, without any multiplier. The multilevel (3 levels) architecture requires 36 adders and 27 shift registers. For 9/7 architectures, the 1-level raster-scan 2-D DWT requires 36 adders and 54 shift registers, while multilevel architectures require 108-adder and 162 shift registers.

Table (3): The total number of adders and shift registers required for the design of the proposed architectures.

Architectures	Number of adder	Number of shift register
Proposed 1-level 2D DWT for 5/3 filter	12	9
Proposed 1-level 2D DWT for 9/7 filter	36	27
Proposed multilevel (3 levels) architecture for 5/3 filter	36	54
Proposed multilevel (3 levels) architecture for 9/7 filter	108	162

It should be noted that the direct structure uses 4-multipliers and 8 adders [12], while the flipping structure reduces the critical path by releasing the major computation path, but without any hardware overhead [10]. The internal memory size in both direct architecture and flipping architecture is equal the image size (NXN). The proposed architectures need internal memory less than image size as shown in Table 4. This will reduce the complexity of the system because the proposed architectures do not need the memory control unit.

Table (4): A comparison of the 2-D architectures for different architectures.

Architectures	No. of multipliers	No. of adders	Internal memory	Control complicity
Direct	4	8	NXN	Complex
Flipping	4	8	NXN	Simple
Proposed 1-level raster scan 2D DWT for 5/3 filter	0	12	3N+2	Simple
Proposed 1-level raster scan 2D DWT for 9/7 filter	0	36	3N+8	Simple
Proposed multilevel-level (3levels) architecture for 5/3 filter	0	36	7N+6	Simple
Proposed multilevel-level (3levels) architecture for 9/7 filter	0	108	7N+24	Simple

8. Conclusions

This paper has presented a high performance and low memory raster-scan architectures for the 2-D lifting scheme DWT of the 5/3 filter and 9/7 filters. By merging predict and update steps into a single step. The proposed architectures use 3-arithmetic module in 1-level architectures and 9 arithmetic modules in multilevel architectures without any multipliers. The proposed scheme in this paper depends on lifting scheme theory because it is a desirable scheme from point of view of hardware performance and high throughput. The proposed 1-level and multilevel 2-D DWTs have been designed, implemented and tested. The comparison shows that the proposed architectures are also preferable from chip utilization point of view.

References

[1] S. G. Mallat, "A theory for multiresolution signals decomposition the wavelet representation " , IEEE trans. pattern, Vol. 11, No. 7, pp. 674 - 693, July 1989.

[2] K. A. Kotteri, S. Barua, A. E. Bell, and J. E. Carletta, "A comparison of hardware implementations of the biorthogonal 9/7 DWT: convolution versus lifting" IEEE Trans. Circuits Systems II, express briefs, Vol. 52, No. 5, pp. 256-260, May 2005.

[3] C. Chakrabarti, M. Vishwanath, and R. M. Owens, "Architectures for wavelet transforms: A survey", J. VLSI Signal Process., Vol. 14, pp.171–192, 1996.

[4] M. Vishwanath, R. M. Owens, and M. J. Irwin, "VLSI architectures for the discrete wavelet transform," IEEE Trans. Circuits Systems II, Analog Digit. Signal processes,Vol. 2, No. 5, pp. 305–316, May 1995.

[5] C. Chakrabarti and M. Vishwanath, "Efficient realizations of the discrete and continuous wavelet transforms: From single chip implementations to mappings on SIMD array computers," IEEE Trans. Signal Process., Vol. 43, No. 3, pp. 759-771, Mar. 1995.

[6] P. Wu and L. Chen, "An efficient architecture for two-dimensional discrete wavelet transform," IEEE Trans. Circuits Syst. Video Technol., Vol. 11, No. 4, pp. 536–545, April 2001.

[7] M. Weeks and M. Bayoumi, "Discrete wavelet transform: architectures, design and performance issues" J. VLSI Signal Process. Syst., Vol. 35, No. 2, pp. 155–178, 2003.

[8] C. Hung, P. Tseng and L. Chen "Generic RAM-based architectures for two dimensional discrete wavelet transform with line-Based method" IEEE. Transactions on

circuits and systems for video technology, Vol.15, No.7, pp. 910-920, July 2005.
[9] K. Andra, C. Chakrabarti and T. Acharya, "A VLSI architecture for lifting based forward and inverse wavelet transform" IEEE Transaction On Signal Processing, Vol.50, No.4, pp. 966-977, April 2002 .
[10] B. Feiwu and C. Lin, "A high performance and memory – efficient pipeline architecture for the 5/3 and 9/7 discrete wavelet transform of JPEG 2000 codec", IEEE transaction on circuits and systems for video technology, Vol. 15, issue 12, pp. 1615-1628, Dec. 2005.
[11] L. Cheng, D. L. Liang and Z. H. Zhang, "Popular biorthogonal wavelet filters via a lifting scheme and its application in image compression", IEEE proc.-Vis. Image Signal process, Vol. 150, No.4, pp. 227-232, Aug. 2003.
[12] J. M. Jou, Y. H. Shiau and C. C. Liu, "Efficient VLSI architectures for biorthogonal wavelet transform by filter bank and lifting scheme", in proc., IEEE ISCAS, Vol. 2, pp. 529-532, May 2001.
[13] O. Fatemi and S. Bolouki, "Pipeline, memory-efficient and programmable architecture for 2D discrete wavelet transforms using lifting scheme" IEEE Proc.-Circuits Devices syst., Vol. 152, No. 6, pp. 703-708, Dec. 2005.

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